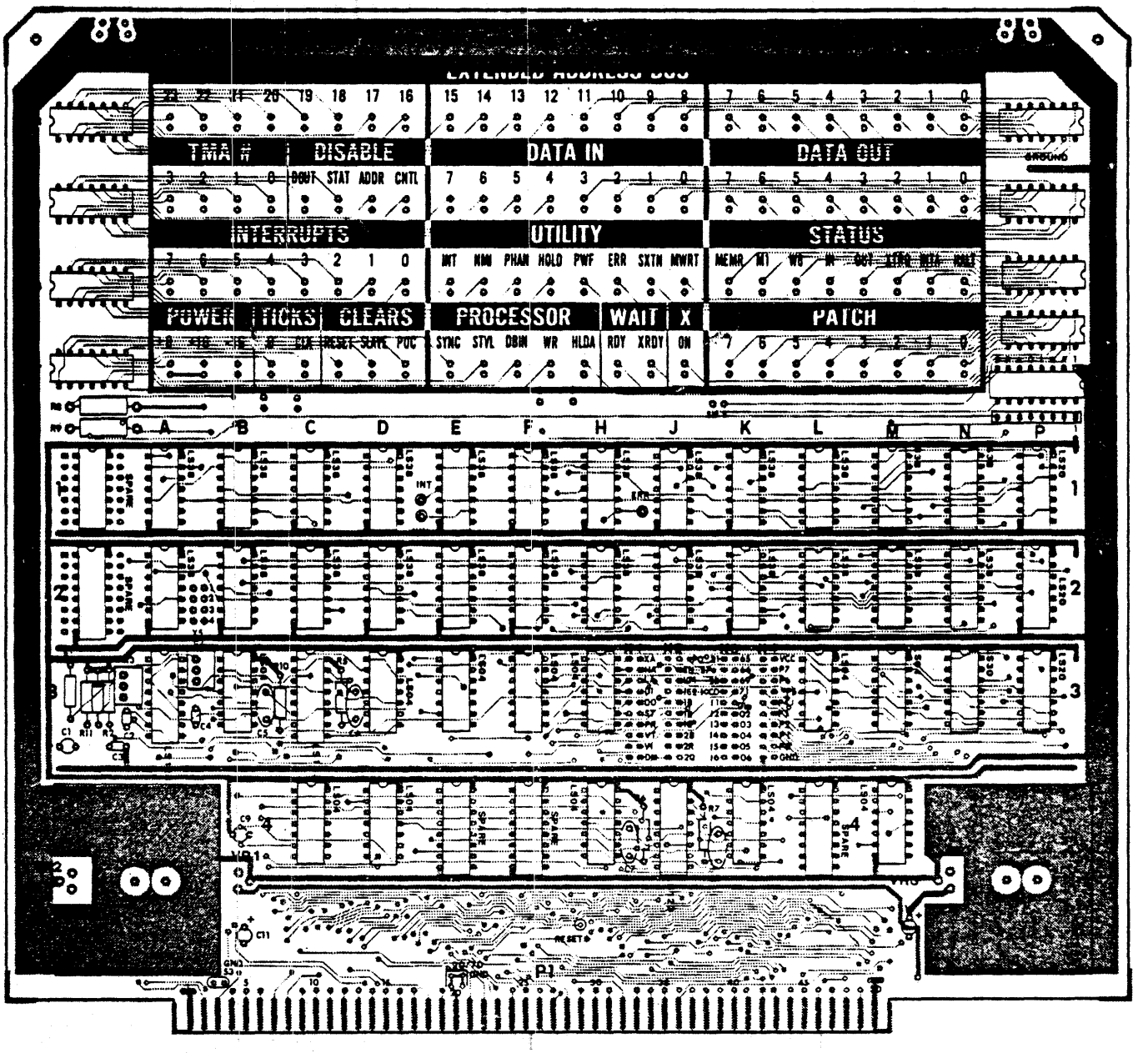
The Bus Probe



JADE
Computer Products

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JADE COMPUTER PRODUCTS

PRESENTS

THE BUS PROBE

HARDWARE MANUAL

TSX-200M

Jade Computer Products
4901 West Rosecrans
Hawthorne, California
90250

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INTRODUCTION

SECTION 1

1.1 SCOPE

This manual contains a complete hardware description of Jade Computer Product's BUS PROBE. It provides the end user with the construction and testing procedures. Also provided are the schematic diagram, traces/silkscreen artwork, and functional description of the circuitry.

1.2 PURPOSE

The BUS PROBE provides an inexpensive tool for troubleshooting of CPU boards, S100 Temporary Bus Masters (such as disk controllers), as well as entire systems. Master boards generate most of the IEEE S100 bus signals. The BUS PROBE allows the user to quickly monitor these IEEE 696 S100 signals. Since very few front panel boards provide for display of the entire S100 bus, and most systems don't have front panels, the BUS PROBE provides a cost effective and easily installed means for troubleshooting.

1.3 DESCRIPTION

The BUS PROBE is a LED display board designed to be inserted into the S100 bus. This board is mostly passive to the S100 bus. It monitors each of the S100 signal lines (with minimal loading) and displays the signal logic level on the corresponding LED. In most cases the LED is ON when the S100 signal is ASSERTED. For address and data lines this is a logic 1 or high TTL level. Note signals like INT* are ASSERTED as a logic 0 or low TTL level. The BUS PROBE is capable of displaying all IEEE 696 S100 signals. This board will also function in most S100 computer systems designed previous to the IEEE specification.

The BUS PROBE can be divided into two sections. The lower half of the board contains the S100 bus interface and display driver circuitry. The lower half of this board is about the same size as a standard S100 board. The upper half of this board contains the display area. The display area has been double silkscreened to enhance the LED display. This section of the board extends above the top of other boards. This makes the display area visible when plugged directly into the S100 bus.

This product allows selective viewing of certain bus cycles. By switch selection the user can display any one or combination of the following bus cycles: M1 instruction fetch, memory read, memory write, port input, and port output.

FUNCTIONAL DESCRIPTION

SECTION 2

2.1 GENERAL

The BUS PROBE is a self-contained display-only panel board for the S100 bus. The 96 LED display is divided into 12 different sections of 8 LEDs each. All LEDs are driven by 74LS38 bus drivers and provide approximately 25 ma of display current for each LED. This provides for a bright display.

The spare inputs of the LS38s for each cluster of 8 LEDS have been connected together to provide a cluster enable line. These cluster enable lines are accessible at jumper block X1. The cluster enable lines are used to provide viewing of selected bus cycles.

2.2 ADDRESS LINES

The full extended address bus can be viewed from this board. Address LEDs 23 thru 0 match the IEEE 696 S100 address lines A23 thru A0. Each LED is on when the corresponding address line is in the high state. Three cluster enable lines control this display.

XADRENB	A23-A16
HADRENB	A15-A08
LADRENB	A07-A00

2.3 DATA LINES

Both the byte wide DATA IN and DATA OUT bus can be viewed from this board. Each LED is on when the corresponding data line is in the high state. The physical layout is such that during word wide data transfers, the entire 16 bits can be viewed in proper order. One cluster enable line controls each half of the display.

DIENB	DI7-DI0
DOENB	DO7-DO0

2.4 TMA AND DISABLE

Temporary Master Access lines can be viewed from this board. Each LED is on when the corresponding bus line is in the low state. DMAENB controls this cluster.

2.5 STATUS

All eight IEEE status lines can be viewed from this board. Each LED is on when the corresponding bus line is in the asserted state, whether that is high or low. STATENB- controls this cluster.

2.6 UTILITY

Eight various IEEE S100 bus signals have been grouped together in this cluster: INT*, NMI*, PHAN*, HOLD*, PWF*, ERR*, SIXTN*, and MWRT. Each LED is on when the corresponding bus line is asserted (MWRT is the only line asserted high).

2.7 INTERRUPTS

All eight vector interrupt request lines VI7* thru VI0* can be viewed from this board as INTERRUPTS 7 thru 0. Each LED is on when the corresponding bus line is in the low state (asserted). VIENB controls this cluster.

2.8 POWER

The three bus voltages, +8 volts, +16 volts, and -16 volts, each drive a corresponding LED directly thru a series limiting resistor. This provides a means to verify bus voltages.

2.9 TICKS

Two LEDs are provided each with a one-shot to monitor bus clocks PHI and CLK. A failure in either clock will show with the corresponding LED off. These two are the only signals that are not directly viewed.

2.10 CLEARS

RESET*, SLAVE CLEAR*, and POC* can be viewed from this board. Each LED is on when the corresponding bus line is asserted low.

2.11 PROCESSOR

The five processor signals pSYNC, pSTVAL*, pDBIN, pWR*, and pHLDA can be viewed on this board. Each LED is on when the corresponding bus line is asserted (either high or low).

2.12 WAIT

Both RDY and XRDY can be viewed from this board. These LEDs are on when the corresponding bus lines are in the low state. NOTE: these are the only LEDs which respond to the unasserted state.

2.13 PATCH

Eight LEDs with corresponding LS38 drivers are on the BUS PROBE as spare indicators. These have been provided for special user needs. The LS38 driver inputs are connected to jumper block X4.

2.14 SPARES

Five spare IC socket locations have been provided on the BUS PROBE for special user needs. These provide Vcc and Gnd connections so be AWARE!

Two spare switch locations have been provided on the top edge of the BUS PROBE. These mountings are for CUTLER-HAMMER subminiature printed circuit board switches. Foils on the solder side of the PCB allow connections to be made below the display area.

LEFT	CENTER	RIGHT	PART NMBR
ON	NONE	ON	SF6TCX392
ON	NONE	TEMP	SF6TGX392
TEMP	NONE	ON	SF6TEX392
ON	OFF	TEMP	SF6TFX392
TEMP	OFF	ON	SF6TAX392
ON	OFF	ON	SF6TBX392
TEMP	OFF	TEMP	SF6THX392

NONE = NO POSITION, TEMP = MOMENTARY

2.15 SWITCH S1

S1 is used to select which type bus cycles are viewed. It also controls the onboard pulse generator. One position of this switch is left as a spare.

POSITION	POS	FUNCTIONAL DESCRIPTION OF POSITION
'1'	OFF	ALLOWS M1 CYCLES TO BE DISPLAYED
'M'	OFF	ALLOWS MEMORY READ CYCLES TO DISPLAY
'W'	OFF	ALLOWS MEMORY WRITE CYCLES TO DISPLAY
'I'	OFF	ALLOWS PORT INPUT CYCLES TO DISPLAY
'O'	OFF	ALLOWS PORT OUTPUT CYCLES TO DISPLAY
'A'	OFF	ALLOWS ALL BUS ACTIVITY TO DISPLAY
'P'	ON	ENABLES ONBOARD PULSE GENERATOR
'S'		SPARE SWITCH POSITION

The display is enabled if any condition determined by switches 1, M, W, I, O, and A is met.

2.16 JUMPER BLOCKS

The following jumper blocks have been provided for the advanced user to make special modifications to the board.

X1 is where all cluster enable lines are connected.

X2 provides access to a spare 74LS123 dual one-shot.

X3 connects to all the RFU (reserved future use) and NDEF (not defined) lines as declared in IEEE 696 S100 bus specifications.

X4 connects to the LS38 inputs that drive the PATCH LEDs. This jumper block has been wired in the foil to kept these LEDs off until X5 is modified. The user will have to cut some foil links to use the PATCH display.

X5 is a distribution area for the onboard pulse generator. One tap will drive the S100 RESET line (75). Row 1 provides two taps to make connections of your choice. A shunt plug at one of rows 2, 3 or 4 will select which tap to drive.t

2.17 MODIFICATIONS

The warranty for this board applies to boards assembled as described in SECTION 3. Even though this board provides for easy modification, Jade Computer Products can not service modified boards. There would be too many individual variations; besides, our technical facility is set up to test only the standard configurations. As this board is intended to be used by technical individuals, this limited service policy should provide no difficulty.

TO MAKE USE OF WARRANTY, TEST ASSEMBLED KIT OR A&T PRODUCT BEFORE MAKING ANY MODIFICATION.

BOARD ASSEMBLY

SECTION 3

3.1 INTRODUCTION

If you have purchased THE BUS PROBE as a kit, we strongly urge you to read this section before attempting to assemble the board. This board is intended for those people who have had some prior experience with digital electronics and circuit board assembly. If you do not, it is recommended that you find an experienced person to help you with the assembly of the board.

3.2 INSPECTION

Check the parts received against the PARTS LIST (Appendix B). Take special care to correctly identify similar looking parts; resistors, capacitors, and diodes. If any part is missing from your kit, please call Jade's Customer Service Department or your local retail store and report the shortage immediately.

3.3 PREPARATION

Make sure you have the tools ready that are needed for kit assembly. For this board the following items are required:

Soldering iron (25 watts)
Damp sponge (keep solder tip clean)
Rosin core solder (preferably 63/37)
Diagonal cutters
Screwdriver
Exacto knife
Lead former (optional)
Needle-nose pliers
Eye protection

3.4 ASSEMBLY

USE EYE PROTECTION WHILE SOLDERING OR CUTTING

[ ] Install 16 pin IC sockets at location 3A, 3C, and 4J. Solder only pins 1 and 9.

[ ] Install 14 pin IC sockets at location RP1 thru RP8. Solder only pins 1 and 8.

[ ] Install 14 pin IC sockets at locations 1A thru 1P. Solder only pins 1 and 8.

[ ] Install 14 pin IC sockets at locations 2A thru 2P. Solder only pins 1 and 8.

[ ] Install 14 pin IC sockets at location 3B.
Install 14 pin IC sockets at locations 3D thru 3H.
Install 14 pin IC sockets at locations 3L thru 3P.
Solder only pins 1 and 8.

[ ] Install 14 pin IC sockets at locations 4C, 4D, 4H, 4K, and 4M. Solder only pins 1 and 8.

[ ] Carefully inspect the printed circuit board (PCB) to determine that all IC sockets are down flat against the PCB. If you find any that are not flat against the PCB, heat the solder joints of the IC pins while pressing the IC socket down.

[ ] Now that all IC sockets are flat against the PCB, turn the PCB solder side up. Inspect each IC area to make sure all IC socket pins are sticking thru the PCB holes. IC sockets are more difficult to remove after the entire IC has been soldered in. Remove any socket not installed correctly, straighten the pin, and re-insert.

[ ] Solder all IC socket pins.

NUMBERS IN PARENTHESIS DENOTE PHYSICAL LOCATION ON PCB

[ ] Install the 5.1K 1/4 W (Green/Brown/Red) resistors at the following locations:

[ ] R1 (3A) [ ] R11 (3A)

[ ] Install 33K 1/4 W (Orange/Orange/Orange) resistor at R2 (3A).

[ ] Install the 6.8K 1/4 W (Blue/Gray/Red) resistors at the following locations:

[ ] R5 (3C) [ ] R10 (3C)

[ ] Install the 910 ohm 1/2 W (White/Brown/Brown) resistors at R8 and R9 (1A). Allow 1/8 inch between bottom of resistors and the PCB.

[ ] Using a cut resistor lead (you should have a few now) prepare a 0.3" diameter loop and install both ends thru the plate-thru holes silkscreened "GROUND" between RP2 and RP4. This provides for making an easy ground connection to the board.

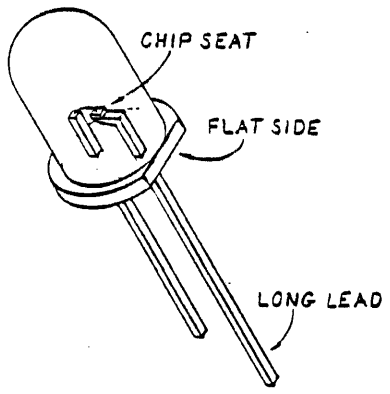
[ ] Install the 100K trimmers at R3 and R4 (3A).

[ ] Install the 3.3K 8 pin SIP resistor pack at RP9 (1P). Observe pin #1 for proper installation.

[ ] Install the 1N914B signal diode at CR1 (3A). Observe banded end of diode matches silk screen.

[ ] **PLEASE READ LED INSTALLATION CAREFULLY**

[ ] Inspect the bottom surface of each LED for molding defects. Remove any surface irregularities with an EXACTO knife to ensure that the LEDs will seat flat on the PCB surface. Be sure to check that the leads have no meniscus from the LED encapsulation.



[ ] Install 24 LEDs along one row of the display area. Be sure that the longer lead of each LED is installed in the hole toward the S100 connector side of the PCB. Only solder one lead of each LED.

[ ] TAKE THE TIME TO CAREFULLY POSITION EACH LED FOR A UNIFORM ROW OF WELL-ALIGNED LEDs. This is very easy to do with only one lead soldered in. NOW INSPECT EACH LED to make sure the flat part of the LED rim is facing toward the S-100 connector.

[ ] Solder the second lead of each LED. Cut the leads off the LEDs.

[ ] Repeat the last three steps for each individual row of LEDs.

BE AWARE OF CAPACITOR SUBSTITUTIONS. Check PARTS LIST for acceptable range of part values.

[ ] Install 4.7 uf 10 volt tantalum capacitors at the following locations. Be careful of plate-thru-holes near C9. OBSERVE CAPACITOR POLARITY!

[ ] C1 (3A) [ ] C9 (4B) [ ] C10 (4M)

[ ] Install 4.7 uf 25 volt tantalum capacitor at C11 (4B). OBSERVE POLARITY.

[ ] Install 3.3 uf 10 volt tantalum cpacitor at C4 (3B). The positive lead is toward trimmer R4.

[ ] Install 0.33 uf 10 volt tantalum capacitor at C2 (3A). The positive lead is toward trimmer R3.

[ ] Install 0.1 uf monolithic capacitor at C3 (3A).

[ ] Install 33 pf mica capacitors at C5 and C6 (3C).

[ ] Prepare two each four-pin strips from the 36 pin header strip. Install these at X5. Insert four shunt plugs across the two strips to maintain alignment while soldering.

[ ] Prepare leads of 7805 regulator for mounting at VR3. Install 7805 on heat sink using #4 hardware set. Insert screw from solder side of PCB. Solder mounted 7805.

[ ] Prepare leads of two 7805 regulators for mounting at VR1 and VR2. Install 7805s on heat sink using two sets #4 hardware. Insert screws from solder side of PCB. Solder mounted 7805s.

[ ] OPTIONAL STEP #1. Install THE 2x10 block header-pins at X1 thru X4 (3J-3K). USE A MINIMUM OF SOLDER. This will prevent INTERCONNECTIONS from being covered with solder. You may desire to cut these during board modification.

Consistent with the IEEE-696 S100 Bus standard, this board connects S100 bus pins #20, 53, and 70 to ground (0 volts). If desired, for use with non standard bus configurations where these lines serve a specific function, these connections to ground may be cut with header pins and jumpers installed for maximum adaptability.

[ ] OPTIONAL STEP #2. On solder side of board cut trace between the two pads immediately above and connected to S100 pin #53. Prepare a 2x1 header strip and install on component side of PCB in silk screened area "53".

Locate on the component side of board immediately above pin #20 the "20/70 GND" silkscreen block. Cut both vertical traces. Install 2 each 2x1 header strips, using 2 shunt plugs to hold alignment between the 2 strips.

[ ] Clean flux from board. Be sure to read and follow manufacturers instructions when using flux cleaners.

[ ] Install switch at S1 (1P). Be sure each switch is OPEN before soldering.

[ ] Install the DIP resistor networks at locations RP1 thru RP8. Observe pin #1 alignment. The silkscreen outline indicates the pin #1 side with an indent.

[ ] Install ICs at all 43 locations. Match the IC number with the silkscreen which identifies each socket location.

This completes the assembly phase of THE BUS PROBE.

TESTING THE BUS PROBE

SECTION 4

4.1 INTRODUCTION

The BUS PROBE can be tested with a minimum of equipment. This section presents a detailed check-out of the BUS PROBE using a voltmeter, a grounding wire, the BUS PROBE itself, and an S100 mainframe. Due to the nature of this board, most test results are taken from the BUS PROBE display area. More advanced tests are described which make use of your system's monitor or operating system.

4.2 INITIAL TESTS

[ ] Turn your mainframe power switch off. Remove all cards from the S-100 mainframe. At this time you should check the motherboard to see that it is free from any lost parts that might have fallen upon it. Insert the Bus Probe into an S-100 card slot. In front of the BUS PROBE insert an S-100 extender card. All positions of S1 should be off.

[ ] Turn mainframe power on. Measure the output voltage of the three regulators. Each should be between 4.8 and 5.2 volts. A ground point is located between RP2 and RP4.

- [ ] Test VR1 at IC 1A pin #14.
- [ ] Test VR2 at RP1 pin #14.
- [ ] Test VR3 at RP2 pin #14.

[ ] Now inspect the BUS PROBE display area. The following is a list of those LEDs which should be on.

- [ ] ADDRESS: All address lines A23 thru A0
- [ ] DATA IN: All DATA IN 7 thru 0
- [ ] DATA OUT: All DATA OUT 7 thru 0
- [ ] STATUS: sMEMR, sM1, sIN, sOUT, sINTA, sHALT
- [ ] PROCESSOR: pSYNC, pDBIN, pHLDA
- [ ] UTILITY: MWRT
- [ ] POWER: +8 VOLTS, +16 VOLTS, -16 VOLTS

4.3 GROUND TEST

The following procedure checks the individual LEDs and the driver IC for proper function. These checks are performed by grounding each individual SIGNAL line of the S100 bus. BE CAUTIONED: Do not ground pins 1, 2, 51, or 52 as these are IEEE S100 power lines. The safety resistor will get hot very quickly (toasty fingers).

[ ] Prepare a testing cable about 18" long. One end should be soldered to an alligator clip. The other end should be soldered to a 15 ohm 3 watt resistor. The free lead of the resistor will function as the test probe tip. Cut probe tip lead to 1" for ease of use. Connect the alligator clip to the ground point located between RP2 and RP4 of the BUS PROBE.

[ ] Using the ground wire, touch each of the following S-100 bus pins on the top connector of the extender card. Verify the corresponding BUS PROBE indication.

PIN	DISPLAY	INDICATION	PIN	DISPLAY	INDICATION
3	XRDY	turns on	29	A5	turns off
4	VI0*	turns on	30	A4	turns off
5	VI1*	turns on	31	A3	turns off
6	VI2*	turns on	32	A15	turns off
7	VI3*	turns on	33	A12	turns off
8	VI4*	turns on	34	A9	turns off
9	VI5*	turns on	35	DO1	turns off
10	VI6*	turns on	36	DO0	turns off
11	VI7*	turns on	37	A10	turns off
12	NMI*	turns on	38	DO4	turns off
13	PWRFAIL*	turns on	39	DO5	turns off
14	DMA3*	turns on	40	DO6	turns off
15	A18	turns off	41	DI2	turns off
16	A16	turns off	42	DI3	turns off
17	A17	turns off	43	DI7	turns off
18	SDSB*	turns on	44	sM1	turns on
19	CDSB*	turns on	45	sOUT	turns on
20	0 Volt	NO EFFECT	46	sINP	turns on
21	RFU	NO EFFECT	47	sMEMR	turns on
22	ADSB*	turns on	48	sHLTA	turns on
23	DODSB*	turns on	49	CLOCK	NO EFFECT
24	PHI	NO EFFECT	50	0 Volt	NO EFFECT
25	pSTVAL*	turns on			
26	pHLDA	turns off	53	0 Volt	NO EFFECT
27	RFU	NO EFFECT	54	SLV CLR*	turns on
28	RFU	NO EFFECT	55	TMA0*	turns on

PIN	DISPLAY INDICATION		PIN	DISPLAY INDICATION	
56	TMA1*	turns on	79	A0	turns off
57	TMA2*	turns on	80	A1	turns off
58	sXTRQ*	turns on	81	A2	turns off
59	A19	turns off	82	A6	turns off
60	SIXTN*	turns on	83	A7	turns off
61	A20	turns off	84	A8	turns off
62	A21	turns off	85	A13	turns off
63	A22	turns off	86	A14	turns off
64	A23	turns off	87	A11	turns off
65	NDEF	NO EFFECT	88	DO2	turns off
66	NDEF	NO EFFECT	89	DO3	turns off
67	PHANTOM*	turns on	90	DO7	turns off
68	MWRT	turns off	91	DI4	turns off
69	RFU	NO EFFECT	92	DI5	turns off
70	0 Volt	NO EFFECT	93	DI6	turns off
71	NDEF	NO EFFECT	94	DI1	turns off
72	RDY	turns on	95	DI0	turns off
73	INT*	turns on	96	sINTA	turns off
74	HOLD*	turns on	97	sWO*	turns on
75	RESET*	turns on	98	ERROR*	turns on
76	pSYNC	turns off	99	POC*	turns on
77	pWR*	turns on	100	0 Volt	NO EFFECT
78	pDBIN	turns off			

[ ] Turn mainframe power off. Wait for power supply to discharge. Now remove the BUS PROBE and insert into the extender card.

[ ] Turn mainframe power on. Using the ground wire, touch each of the following BUS PROBE IC pins. Verify the corresponding BUS PROBE indication.

IC-PIN	DISPLAY INDICATION	
1K-3	PATCH 7	turns on
1K-11	PATCH 6	turns on
1L-3	PATCH 5	turns on
1L-11	PATCH 4	turns on
1M-3	PATCH 3	turns on
1M-11	PATCH 2	turns on
1N-3	PATCH 1	turns on
1N-11	PATCH 0	turns on

4.4 CYCLE DISPLAY

The following procedure checks the BUS PROBE ability to view selective bus cycles. The software is written in 8080 code so as to operatate with the 8080, 8085, and the Z80 microprocessors. Similar programs can be wriiten by those users who have other microprocessors. Use TSX/PGM1 as an example.

The following programs require system memory from 0100H to 0157H. This is a minimum, those systems having more memory are acceptable. TSX/PGM1 can be modified to avoid any I/O which could affect the users I/O address space. Pick unused port numbers.

[ ] Turn your mainframe power switch off. Insert your system card set. Install the BUS PROBE into your mainframe.

[ ] Turn your mainframe power switch on. Enter program TSX/PGM1 into your computer and execute it. The following listing contains the needed HEX CODE.

```
                ;*********************************************
                ;   BUS PROBE CYCLES DISPLAY  -  TSX/PGM1    *
                ;*********************************************
                ; PROGRAM EXECUTES DIFFERENT MACHINE CYCLES *
                ; TO ENABLE TESTING  THE BUS PROBE'S  CYCLE *
                ; SELECTION CIRCUIT  -  OCT 27, 1981  -  SK *
                ;*********************************************

0100                    ORG     0100H       ;CP/M TPA AT 0100H

                ;*****( PROGRAM BEGINS )**********************

0100 2100AA             LXI     H,0AA00H    ;HL SET TO AA00H.
0103 3E0F       REPEAT: MVI     A,0FH       ;LOW NIBBLE SET.
0105 D333               OUT     33H         ;OUT TO PORT 33H.
0107 77                 MOV     M,A         ;WRITE REG TO MEM.
0108 DB00               IN      00H         ;INPUT FROM 00H.
010A C30301             JMP     REPEAT      ;ENDLESS LOOP.
010D                    END
```

TEST M1 CYCLE.

[ ] Set S1 to the following settings:

S is OFF	P is OFF	A is ON	O is ON
I is ON	W is ON	R is ON	1 is OFF

Verify: Address bits A15 thru A8 are '00000001' or 01 hex. Status M1 and MEMR are on.

TEST MEMORY READ CYCLE

[ ] Alter S1 settings: R to OFF 1 to ON

Verify: Address bits A15 thru A8 are '00000001' or 01 hex.
Status MEMR is on.

TEST MEMORY WRITE CYCLE.

[ ] Alter S1 settings: W to OFF R to ON

Verify: Address bits A15 thru A8 are '10101010' or AA hex.
Data bits DO7 thru DO0 are '00001111' or 0F hex.
Status WO is on.

TEST PORT INPUT CYCLE.

[ ] Alter S1 settings: I to OFF W to ON

Verify: Address bits A7 thru A0 are all off.
Status IN is on.

TEST PORT OUTPUT CYCLE

[ ] Alter S1 settings: O to OFF I to ON

Verify: Address bits A7 thru A0 are '00110011' or 33 hex.
Data bits DO7 thru DO0 are '00001111' or 0F hex.
Status OUT is on.

THIS COMPLETES THE TESTING.

4.5 SCAN DISPLAYS

TSX/PGM2 and TSX/PGM3 are optional test programs. TSX/PGM2 scans the DATA OUT leds. TSX/PGM3 scans the ADDRESS leds. For either program the BUS PROBE should be set to view only the MEMORY WRITE bus cycle.

```
                ;*********************************************
                ;   BUS PROBE DISPLAY SCANNER  -  10/28/81   *
                ;   JADE COMPUTER PRODUCTS  - TSX/PGM2.ASM   *
                ;*********************************************
                ;  SCANS ONE LED AT A TIME IN DATA OUT AREA.*
                ;  DISPLAY. ALSO ALTERNATELY DISPLAYS EVERY *
                ;  OTHER ADDRESS BIT LED.                   *
                ;*****************************************(SK)**

0100                    ORG     0100H   ;CP/M TPA AT 0100H

0B00 =          TIMER   EQU     0B00H

                ;*****( PROGRAM BEGINS )**********************

0100 00         BEGIN:  NOP             ;ONE IDLE BYTE.
0101 215555             LXI     H,5555H ;EVERY OTHER BIT HL.
0104 0E80               MVI     C,80H   ;SET THE 7 BIT IN C.

                ;*****( ALTER HL REG )************************

0106 7C         AGAIN:  MOV     A,H     ;LD ACUM WITH H REG.
0107 2F                 CMA             ;COMPLEMENT A REG.
0108 67                 MOV     H,A     ;BACK TO H REG.
0109 6F                 MOV     L,A     ;ALSO TO L REG.

                ;*****( ROTATE DATA TO BE WRITTEN )***********

010A 79                 MOV     A,C     ;MOVE C TO A REG.
010B 0F                 RRC             ;ROTATE RIGHT
010C 4F                 MOV     C,A     ;UPDATE C REG.

                ;*****( WRITE A REG TO MEMORY )**************

010D 11000B             LXI     D,TIMER ;LOAD TIMER VALUE
0110 71         WR$AGN: MOV     M,C     ;WRITE MEMORY
0111 71                 MOV     M,C     ;WRITE MEMORY
0112 71                 MOV     M,C     ;WRITE MEMORY
0113 71                 MOV     M,C     ;WRITE MEMORY
0114 71                 MOV     M,C     ;WRITE MEMORY
0115 71                 MOV     M,C     ;WRITE MEMORY
0116 71                 MOV     M,C     ;WRITE MEMORY
0117 71                 MOV     M,C     ;WRITE MEMORY

                ;*********************************************

0118 1B                 DCX     D       ;DEC LOOP CNTR
0119 7A                 MOV     A,D     ;GET A REG.
011A B3                 ORA     E       ;OR IN E REG
011B C21001             JNZ     WR$AGN  ;NOT 0, WRITE AGAIN.
011E C30601             JMP     AGAIN   ;ENDLESS LOOP.

                ;*********************************************
0121                    END
```

```
                        ;*******************************************
                        ;   BUS PROBE DISPLAY SCANNER 2 - 10/28/81  *
                        ;   JADE COMPUTER PRODUCTS  - TSX/PGM3.ASM  *
                        ;*******************************************
                        ;  SCANS THE 16 BIT ADDRESS BUS WITH  *
                        ;  PATTERNS.  ALSO FLASHES THE DATA OUT BUS *
                        ;*************************************(SK)**

0100                            ORG     0100H   ;CP/M TPA AT 0100H

0700 =                  TIMER   EQU     0700H

                        ;*****( PROGRAM BEGINS )**********************

0100 00                 BEGIN:  NOP             ;ONE IDLE BYTE.
0101 315801                     LXI     SP,STK$TP       ;STACK ADDR.
0104 0E00                       MVI     C,0             ;ZERO C REG.

                        ;*****( PASS 1 - WALK 1 BIT ON )*************

0106 210100             P1$BGN: LXI     H,0001H ;SET ZERO BIT IN HL.
0109 CD3F01             P1$NXT: CALL    BURST
010C 7C                         MOV     A,H     ;GET H REG.
010D B5                         ORA     L       ;OR IN L REG (SET ZF)
010E 29                         DAD     H       ;HL SHIFT LFT (NO CC)
010F C20901                     JNZ     P1$NXT  ;REPEAT NOT ZERO.

                        ;*****( PASS 2 - FILL ACROSS WITH 1'S )******

0112 210100                     LXI     H,0001H ;SET ZERO BIT IN HL.
0115 CD3F01             P2$NXT: CALL    BURST
0118 7C                         MOV     A,H     ;GET H REG.
0119 A5                         ANA     L       ;OR IN L REG (SET ZF)
011A 2F                         CMA             ;COMPLEMENT
011B B7                         ORA     A       ;SET ZERO FLAG.
011C 29                         DAD     H       ;HL SHIFT LFT (NO CC)
011D 23                         INX     H       ;FILL IN LOW ORDER.
011E C21501                     JNZ     P2$NXT  ;REPEAT NOT ZERO.

                        ;*****( PASS 3 - WALK 0 BIT ACROSS )*********

0121 21FEFF             P3$BGN: LXI     H,0FFFEH ;SET ZERO BIT IN HL.
0124 CD3F01             P3$NXT: CALL    BURST
0127 7C                         MOV     A,H     ;GET H REG.
0128 A5                         ANA     L       ;AND IN L REG.
0129 2F                         CMA             ;COMPLEMENT A REG.
012A B7                         ORA     A       ;SET ZERO FLAG
012B 29                         DAD     H       ;HL SHIFT LEFT.
012C 23                         INX     H       ;SET LOW ORDER BIT.
012D C22401                     JNZ     P3$NXT  ;REPEAT NOT ZERO.

                        ;*****( PASS 4 - FILL ACROSS WITH 0'S )******
```

```
0130 21FEFF            LXI     H,0FFFEH ;SET ZERO BIT IN HL.
0133 CD3F01  P4$NXT:   CALL    BURST
0136 7C                MOV     A,H      ;GET H REG.
0137 B5                ORA     L        ;AND IN L REG.
0138 29                DAD     H        ;HL SHIFT LEFT.
0139 C23301            JNZ     P4$NXT   ;REPEAT NOT ZERO.

013C C30601            JMP     P1$BGN   ;REPEAT PROGRAM.

               ;*****( PROBE DISPLAY DRIVER )***************

013F 110007  BURST:    LXI     D,TIMER  ;LOAD TIMER VALUE
0142 71      REPEAT:   MOV     M,C      ;WRITE MEMORY
0143 71                MOV     M,C      ;WRITE MEMORY
0144 71                MOV     M,C      ;WRITE MEMORY
0145 71                MOV     M,C      ;WRITE MEMORY
0146 71                MOV     M,C      ;WRITE MEMORY
0147 71                MOV     M,C      ;WRITE MEMORY
0148 71                MOV     M,C      ;WRITE MEMORY
0149 71                MOV     M,C      ;WRITE MEMORY

014A 1B                DCX     D        ;DEC LOOP CNTR
014B 7A                MOV     A,D      ;GET A REG.
014C B3                ORA     E        ;OR IN E REG
014D C24201            JNZ     REPEAT   ;NOT 0, WRITE AGAIN.

0150 79                MOV     A,C      ;GET C REG.
0151 2F                CMA              ;COMPLEMENT.
0152 4F                MOV     C,A      ;RETURN C REG.
0153 C9                RET              ;RETURN TO CALLER.

               ;*********************************************

0154 00000000          DW      0,0      ;STACK AREA.
0158 =       STK$TP    EQU     $        ;TOP OF STACK.
0158                   END              ;END PROGRAM.
```

APPENDIX A

IEEE 696 S100 BUS PIN LIST

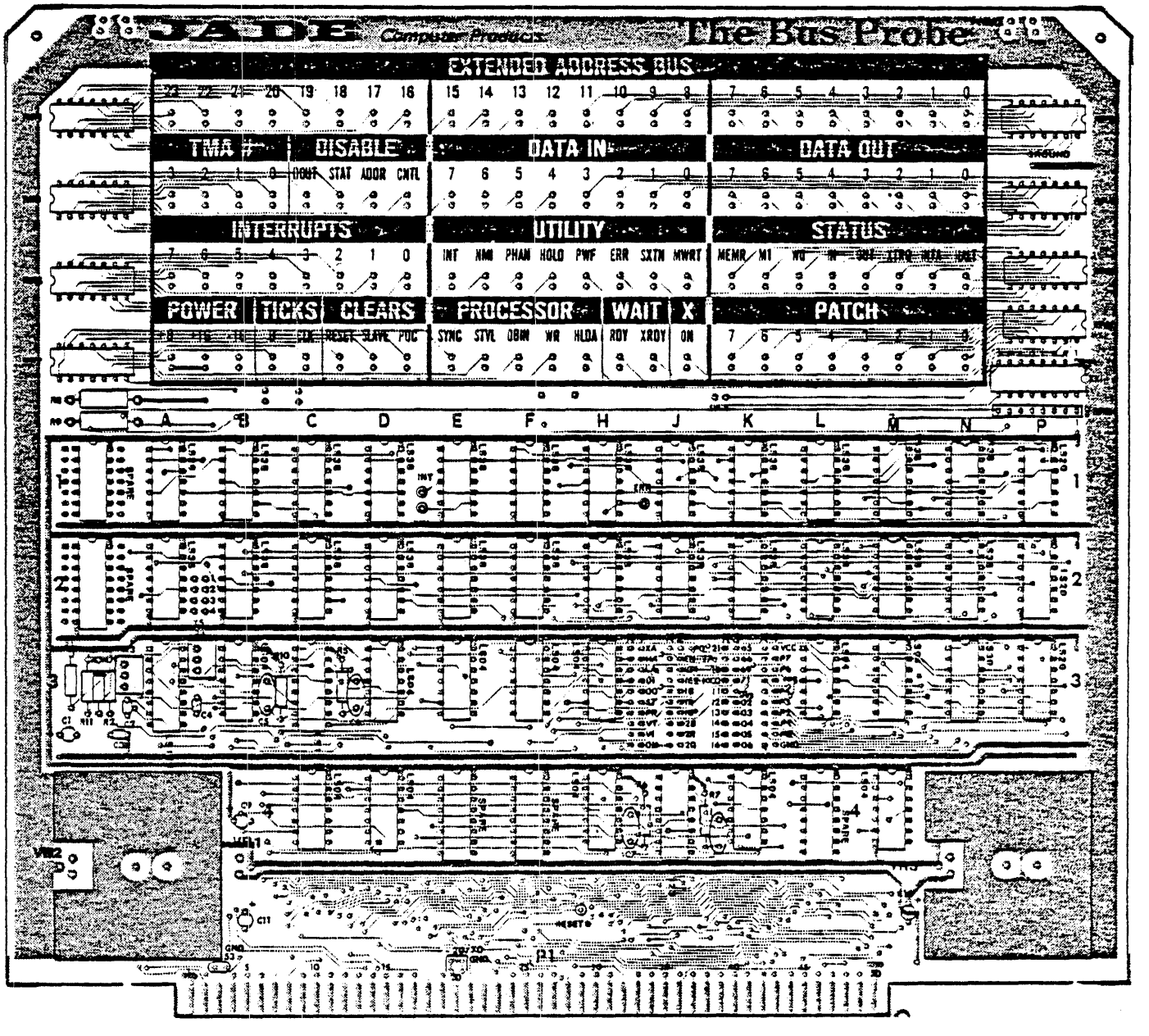
PIN	FUNCTION	PIN	FUNCTION
1	+8 Volts	51	+8 Volts
2	+16 Volts	52	-16 Volts
3	XRDY	53	GND
4	VI0*	54	SLAVE CLR*
5	VI1*	55	TMA0*
6	VI2*	56	TMA1*
7	VI3*	57	TMA2*
8	VI4*	58	sXTRQ*
9	VI5*	59	A19
10	VI6*	60	SIXTN*
11	VI7*	61	A20
12	NMI*	62	A21
13	PWRFAIL*	63	A22
14	DMA3*	64	A23
15	A18	65	NDEF
16	A16	66	NDEF
17	A17	67	PHANTOM*
18	SDSB*	68	MWRT
19	CDSB*	69	RFU
20	0 Volts	70	0 Volts
21	RFU	71	NDEF
22	ADSB*	72	RDY
23	DODSB*	73	INT*
24	PHI	74	HOLD*
25	pSTVAL*	75	RESET*
26	pHLDA	76	pSYNC
27	RFU	77	pWR*
28	RFU	78	pDBIN
29	A5	79	A0
30	A4	80	A1
31	A3	81	A2
32	A15	82	A6
33	A12	83	A7
34	A9	84	A8
35	DO1	85	A13
36	DO0	86	A14
37	A10	87	A11
38	DO4	88	DO2
39	DO5	89	DO3
40	DO6	90	DO7
41	DI2	91	DI4
42	DI3	92	DI5
43	DI7	93	DI6
44	sM1	94	DI1
45	sOUT	95	DI0
46	sINP	96	sINTA
47	sMEMR	97	sWO*
48	sHLTA	98	ERROR*
49	CLOCK	99	POC*
50	0 Volts	100	0 Volts

ITEM	QTY	JADE PART NO.	DESCRIPTION
1	1	TSX-200B	PC BOARD, BUS PROBE
2	1	TSX-200M	MANUAL, BUS PROBE
3	2	CAS-330P500	Capacitor, 33 pf. mica
4	1	CAL-104P500	Capacitor, 0.1 uf. monolithic
5	3	CAT-475P100	Capacitor, 4.7 uf 10 v tant. (4.7 thru 10UF, > or = 10 V)
6	1	CAT-685P200	Capacitor, 6.8 uf 25 v tant. (4.7 thru 10UF, > or = 25 V)
7	1	CAT-334P100	Capacitor, 0.33 uf 10 v tant.
8	1	CAT-335P100	Capacitor, 3.3 uf 10 v tant.
9	1	CNM-111362	1X36 Header Strip
10	4	CNM-121092	2X10 Header Strip
11	10	CNF-12020	Shunt plug
12	2	HDH-34304	Massive TO-220 heat sink
13	3	ICL-LM340T5	+5V TO-220 voltage reg.
14	4	NO P/N	#4 screw, nut, and washer
15	12	ICT-74LS04	Hex inverter
16	3	ICT-74LS20	Dual 4 input nand gate
17	1	ICT-74LS30	8 input nand gate
18	24	ICT-74LS38	Quad 2 input nand buffer
19	3	ICT-74LS123	Dual one-shot
20	8	RCD-1413150.0	Resistor Pack, 150 Ohms 14 pin / 13 resistors.
21	1	RCS-08073.30K	Resistor Pack, 3.3K 8 pin / 7 resistor SIP.
22	1	RCQ-33.0K	Resistor, 1/4 W 33.0 K
23	2	RCQ-6.80K	Resistor, 1/4 W 6.8K
24	2	RCQ-5.10K	Resistor, 1/4 W 5.1K
25	2	RCH-910.0	Resistor, 1/2 W 910 Ohms
26	2	RCT-10440	Resistor, 100K cermet trimmer
27	100	SEO-5053S	Red light emitting diode.
28	1	SED-1N914B	Silicon signal diode.
29	3	SKL-1601	IC Socket, 16 pin
30	48	SKL-1401	IC Socket, 14 pin
31	1	SWD-108	8 SPST DIP switch
32	1	RCR-15.00	Resistor, 3 W 15 Ohm
33	1	NO P/N	24" length hookup wire
34	1	HDX-00100	Alligator clip, small

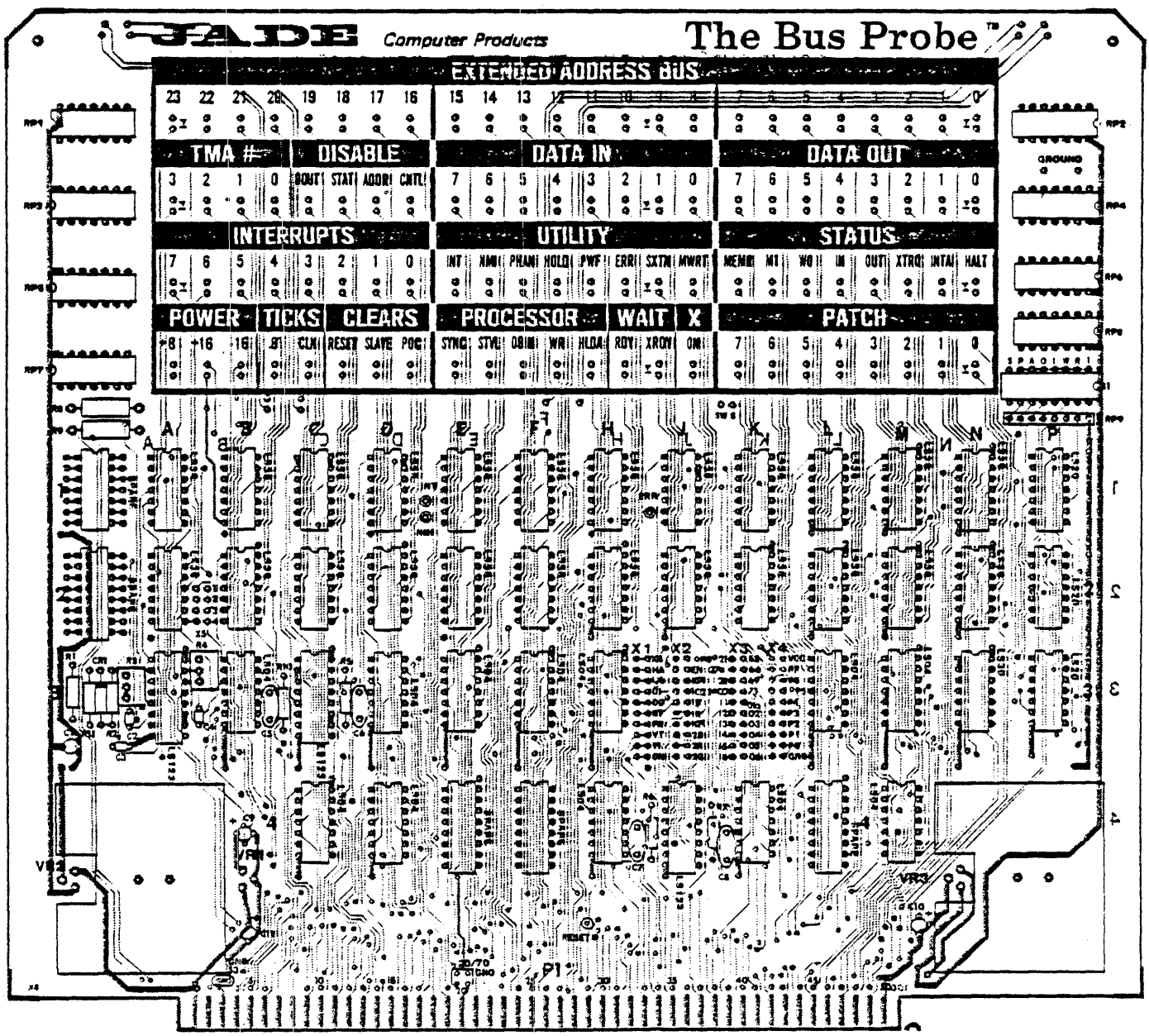
APPENDIX C

Component Side - Front View

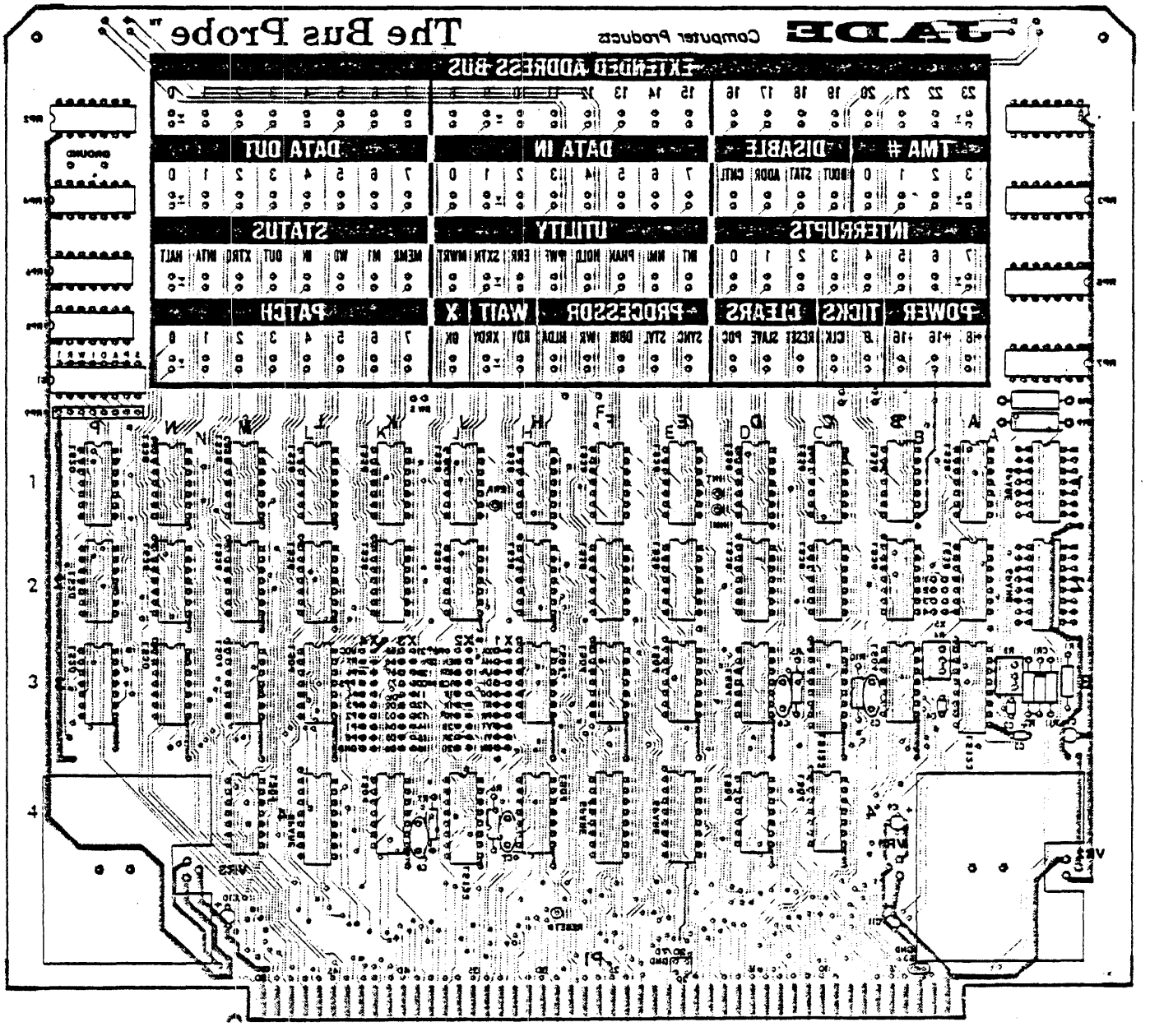
In the following prints the silkscreen is shown as solid dark while the foil patterns are shown in halftone. Both sides of the BUS PROBE are presented as both true and reverse images. Hopefully this presentation will allow the user greater ease in tracing foils from one side of the board to the other.



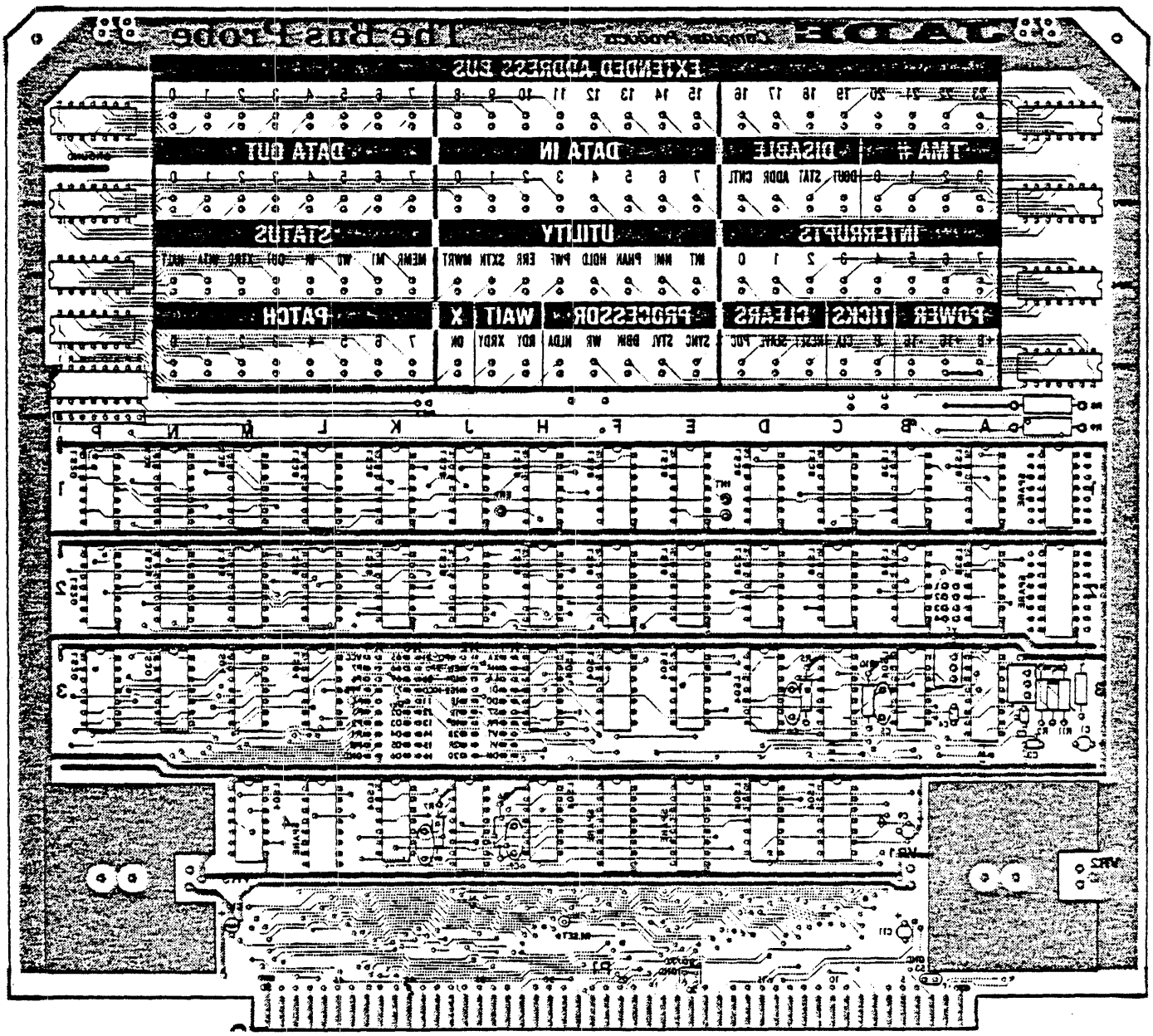
Solder Side - Front View



Component Side - Back View



Solder Side - Back View



This sheet presents some corrections to the first release of the BUS PROBE manual. Please make those corrections to your manual as indicated. Also, some additional information is presented we would like to call your attention to.

- PAGE 12 -

Five pin test indications are in error as declared in the GROUND TEST procedure. The proper test indication for S100 pins 44, 45, 46, 47, and 48 should all be "turns off".

PIN	DISPLAY INDICATION	
44	sM1	turns off
45	sOUT	turns off
46	sINP	turns off
47	sMEMR	turns off
48	sHLTA	turns off

Pin 14 should be labeled as TMA3*. The previously defined DMA signal names has been changed to TMA names (temporary master access).

- SIGNAL NAMES -

All signal names under the STATUS GROUP have the leading "s" removed to allow larger lettering to be used on the silkscreen. This should cause no difficulty as the "s" stands for "status". EXAMPLE: STATUS - MEMR represents the signal sMEMR. This same procedure was followed for all signals under the PROCESSOR heading. PROCESSOR represents the prefix "p".

The STAR designation (*) for negitive signal polarity has been dropped from the silkscreen to allow larger lettering to be used. All STAR'ed signals are displayed so that the LED is on during the asserted signal condition.

The silkscreen TMA disable signal names are easy to understand once explained.

IEEE NAME	SILKSCREEN	IEEE SIGNAL FUNCTION
SDSB* 18	DISABLE - STAT	DISABLES STATUS LINES
CDSB* 19	DISABLE - CNTL	DISABLES CONTROL LINES
ADSB* 22	DISABLE - ADDR	DISABLES ADDRESS LINES
DODSB* 23	DISABLE - DOUT	DISABLES DATA OUT LINES

S100 signal sHLTA appears in the STATUS CLUSTER as HALT.

- CPUs -

Some CPU boards do not generate the sWO* signal (S.D. Sales SBC200 as an example). This inhibits the cycle selection circuit from responding to MEMORY WRITE and PORT OUTPUT cycles. The following modification can be performed which will eliminate the need for the BUS PROBE to monitor sWO*.

1. Lift pin #1 of IC 3P.
2. Lift pin #1 of IC 1P.

An easy way to lift a pin is to unplug the IC, then bend the IC pin up, then insert the IC back into the socket. The selected IC pin is no longer in circuit.

- GROUND PINS -

This item is important enough to repeat. On the BUS PROBE S100 pins #20, 70, and 53 are connected to ground. On some pre-IEEE systems these grounded lines will cause those systems to not function. These connections can be broken. PLEASE follow OPTIONAL STEP #2 in the BUS PROBE manual (SECTION 3 - PAGE 10).

- SCHEMATIC -

For each LED in the BUS PROBE schematic there is a corresponding part designation. This consists of "CR" and a number/letter combination. The numbers correspond to the EXTENDED ADDRESS BUS numbering 23 thru 0. The letters A, B, C, and D correspond to the row. Row A is on top, the EXTENDED ADDRESS BUS row. Row D is on the bottom, the row which includes the POWER LEDs and the PATCH LEDs. An LED labeled CR12C would be under the A12 LED in row C, the UTILITY signal HOLD.

- 64K ADDRESS SPACE -

The EXTENDED ADDRESS LINES A23 thru A16 serve little use on those systems which only use 16 address lines. To turn A23 thru A16 off cut the foil link "XA" on jumper block X1.

- X -

The BUS PROBE panel includes an LED labeled "X". This LED indicates when the cycle selection circuit is inhibiting the display.

JADE would welcome your comments about this board. We are very much interseted in you, our customer, and we want to provide ourselves with some feedback about how you like the product and documentation. Please take a moment to fill out the questionaire and return it to us at the address below.

JADE COMPUTER PRODUCTS
ENGINEERING DEPARTMENT
4901 WEST ROSECRANS
HAWTHORNE, CA 90250

1. Was your BUS PROBE damaged in shipment? YES NO

2. Were any parts missing? YES NO

   If yes, what were they? _____

   _____

3. Was the quality of the material and

   workmanship good? YES NO

4. Did you have any trouble understanding the manual? YES NO

   If so, in what area(s)? _____

   _____

5. Have you encountered problems with the BUS PROBE? YES NO

   If yes, what? _____

   _____

6. Did you solve the problem? YES NO

   If so, how? _____

   _____

   _____

7. Are you satisfied with your BUS PROBE? YES NO

   Why? _____

   _____

SEE OTHER SIDE

8. Do you have any suggestions for improvement? YES NO

If yes, what? _____

_____

9. Other comments? _____

_____

_____

_____

_____

_____

_____

_____

_____

_____

_____

_____

_____

_____

_____

_____

10. NAME: _____

ADDRESS: _____

CITY, STATE: _____

ZIP CODE: _____

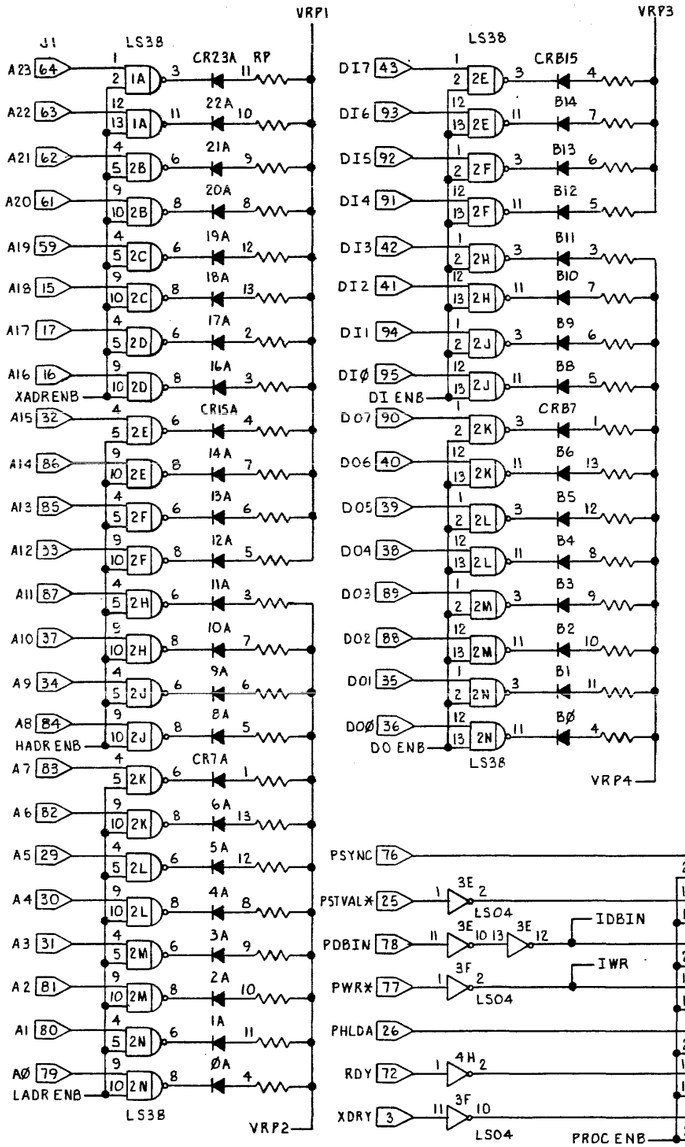
PHONE: _____

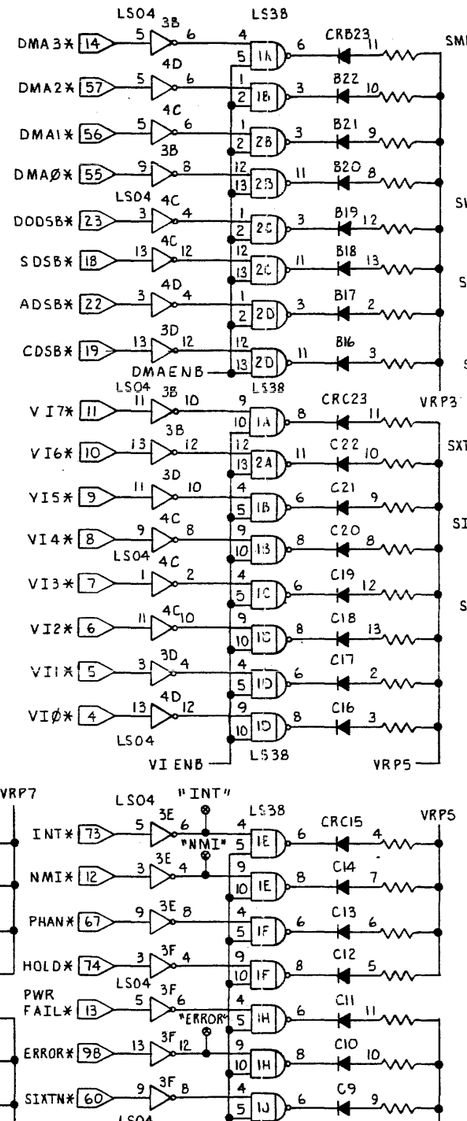
THANK YOU

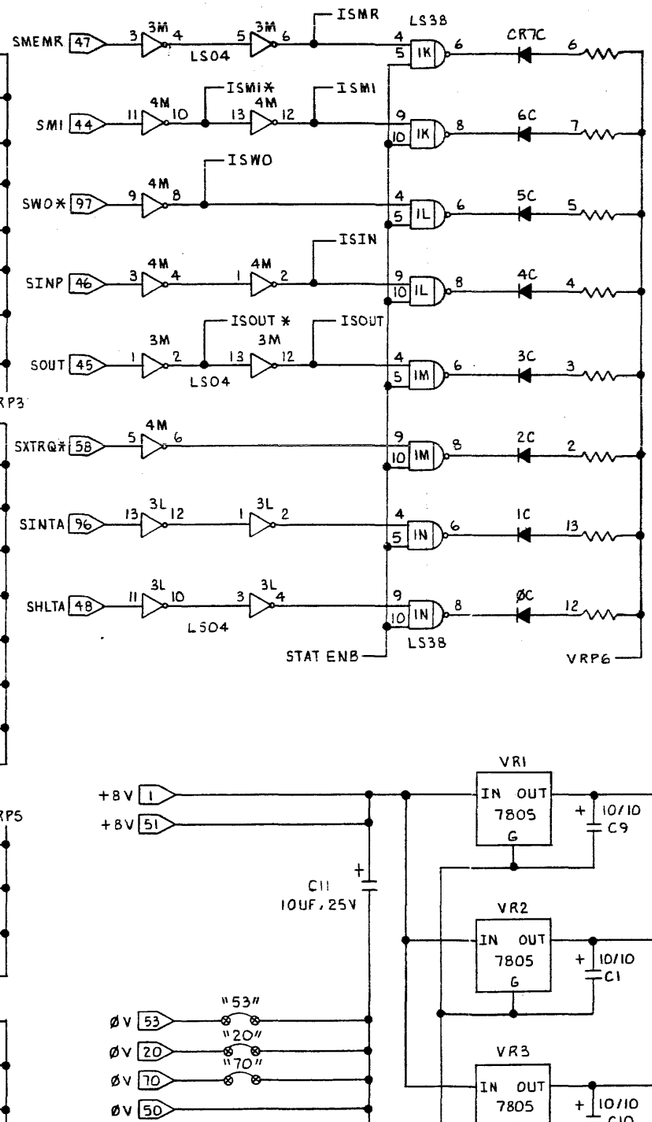
DWG. NO.	SH	REV.
TSX-200	1	C

REVISIONS

ZONE	REV.	DESCRIPTION	DATE	APPROVED







1. —⊗ SYMBOL FOR PLATED THRU HOLE TEST POINT.

NOTES: UNLESS OTHERWISE SPECIFIED.

QTY REQD	FSCM NO.	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±	CONTRACT NO.		JADE Computer Systems
	APPROVALS	DATE	LOGIC DIAGRAM
MATERIAL	DRAWN HAK	11-11-81	THE BUS PROBE
FINISH	CHECKED		
NEXT ASSY / USED ON	ISSUED STAN KUNNIE	11-16-81	SIZE D · FSCM NO. · DWG. NO. TSX-200 · REV. C
APPLICATION	DO NOT SCALE DRAWING		SCALE · SHEET 1 OF 2

TSX-200

DWG. NO.	SH	REV.
TSX - 200	2	C

REVISIONS

ZONE	REV.	DESCRIPTION	DATE	APPROVED

2 x 10 ARRAY X3

2 x 10 ARRAY X4

2 x 10 ARRAY X1

NOTE: X2 PHYSICALLY OUT OF SEQUENCE USE PIN #5

QTY REQD	FSCM NO.	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS = DECIMALS .XX ± .XXX ± ANGLES =

MATERIAL

FINISH

NEXT ASSY | USED ON

APPLICATION | DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN HAK	11-11-81
CHECKED	
ISSUED STAN GRIMME	11-18-81

JADE Computer Systems

LOGIC DIAGRAM

THE BUS PROBE

SIZE	FSCM NO.	DWG. NO.	REV.
D		TSX - 200	C

SCALE | SHEET 2 OF 2

TSX-200